Reg. No. : .....

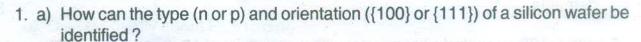
Sixth Semester B.Tech Degree Examination, May 2016 (2008 Scheme)

08.602 : VLSI DESIGN (TA)

Time: 3 Hours

PART-A

Answer all questions. Each question carries 4 marks.



- b) You are asked to pick say, 10 numbers of (sliced) mono-crystalline silicon wafers from an Ingot grown using CZ method. From which portion (top/middle/ bottom) of the ingot, the wafers will be chosen? Justify your answer.
- Write the expressions (derivation not required) for Linear and Parabolic rate constants of a thermal oxidation process. Explain the effect of temperature on these oxidation rate constants.
- Briefly explain the channeling effect in an ion implantation process. Describe the methods to overcome the channeling effect.
- 4. Explain any one of the failure mechanisms of metal contacts with the remedial techniques.
- 5. With the help of switching input and output waveforms of CMOS inverter, how to calculate input rise time, fall time, output rise time, fall time and propagation delay?
- 6. Your friend employs NMOS devices for PUN and PMOS devices for PDN. Show a typical input and output wave transient set. Assume  $V_{DD}=2.5\ V$  and  $V_{TN}=-V_{TP}=0.4V$ .
- 7. Discuss briefly about the VLSI Design Flow.
- Explain the operation of register based multipliers and how it is different from normal array multiplier with its advantages.



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- Explain fault simulation in detail with its types and give an application for each type.
- 10. Compare and contrast SRAM, DRAM and ROM.

## PART-B

Answer any two questions from each Module. Each question carries 10 marks.

## Module - I

- 11. a) With a neat sketch, explain in detail about the Bridgman's method of crystal growth.
  - b) With a neat sketch, explain the process of X-ray lithography with its merits and demerits.
- 12. A p-type<100> oriented silicon wafer with a resistivity of 10 Ω -cm is placed in a wet oxidation system to grow a field oxide of 0.45 μm at 1050° C. Determine the time required to grow the oxide layer. After this oxidation process, a window is opened in the oxide to grow a gate oxide at 1000° C for 20 minutes in dry oxidation. Find the thickness of the gate oxide and the total field oxide. It is given that:
  - i) Rate constants (@ 1050° C-wet) : B = 0.47  $\mu$  m²/hr and B/A = 1.5  $\mu$  m/hr and k = 0 and
  - ii) Rate constants (@ 1000° C-dry) : B = 0.01  $\mu$  m<sup>2</sup>/hr and B/A = 0.06  $\mu$  m/hr and the value k = 0.372 hour.
- 13. Explain in detail about a 2-step thermal diffusion process with required equations. In thermal diffusion, why a 2-step process is required to realize doped layers? Comment on the possibility of realizing shallow junctions with low doping concentrations using a thermal diffusion process.

## Module - II

- 14. Derive an expression for the drain current of an n- channel MOSFET in terms of its geometrical dimensions and terminal voltages. Briefly explain on the design and technological parameters to increase the drain current for fixed terminal voltages.
- 15. Implement the following expression in Table 12.
  - i) static CMOS logic and
  - ii) dynamic logic:  $Y = [(A \times B) + (A \times C \times E) + (D \times E) + (D \times E) + (D \times C \times B)]$ .



- 16. Discuss the various power dissipation components of CMOS circuits. Identify how the following influence the power dissipation:
  - i) Scaling of devices,
  - ii) Operating voltage and
  - iii) Speed of operation.

## Module - III

- 17. For the given logical function  $F = \overline{X}_1 \overline{X}_2 \overline{X}_3 + \overline{X}_1 \overline{X}_2 \overline{X}_3$ , find the minimum number of test vectors to detect the stuck at faults using Boolean difference method.
- 18. a) Draw the circuit diagram of SRAM cell and explain its read write operations.
  - b) Discuss briefly about PLA folding.
- 19. Explain signature analysis in test pattern generation with an example.